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MIC-41

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee : Seong-hoon Lee
Assignee : Micron Technology, Inc.
Patent No. : 6,952,127 B2
Issued : October 4, 2005
Application No. : 10/719,348
Confirmation No. : 3302
Filed : November 21, 2003
For : DIGITAL PHASE MIXERS WITH ENHANCED SPEED
Group Art Unit : 2816
Examiner : Kenneth B. Wells

Certificate
DEC 20 2005
of Correction

New York, New York 10020
December 12, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REQUEST UNDER 37 C.F.R. § 1.322
FOR CERTIFICATE OF CORRECTION

Sir:

Enclosed is one (1) sheet of Form PTO/SB/44 (in duplicate) listing printing errors that have been found in the above-identified patent. The errors are clerical and self-explanatory and their correction does not constitute new matter and requires no reexamination.

DEC 21 2005

The errors are believed to be the responsibility of the U.S. Patent and Trademark Office, and thus no fee is believed to be required in connection with this Request. However, if for any reason a fee is required in connection with this Request, please charge that fee to Deposit Account No. 06-1075, Order No. 002322.0041. A duplicate copy of this Request is enclosed herewith.

Accordingly, patentee and assignee respectfully request that the Patent and Trademark Office issue a Certificate of Correction Under 37 C.F.R. § 1.322.

Respectfully submitted,

Evelyn C. Mak

Evelyn C. Mak
Reg. No. 50,492
Attorney for Patentee
and Assignee

I hereby certify that this
Correspondence is being
deposited with the U.S.
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,952,127 B2
DATED : October 4, 2005
INVENTION : DIGITAL PHASE MIXERS WITH ENHANCED
SPEED

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, line 63: Delete "lo" before "conjunction".

Column 4, line 67: Insert after "signal 306 as" the following --NMOS gate 314 in block 310. The gate of NMOS transistor 332 is coupled to receive complement input signal 302' while the drain is coupled to the drain of PMOS transistor 352.--.

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PATENT NO.: 6,952,127 B2

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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